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09/312,835	05/17/1999	SEUNG-HWAN MOON	06192.0070	3103

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EXAMINER	
KUMAR, SRILAKSHMI K	
ART UNIT	**PAPER NUMBER**
2629	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	04/02/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	09/312,835	MOON, SEUNG-HWAN	
	Examiner	Art Unit	
	Srilakshmi K. Kumar	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 January 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 and 4-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1, 4-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

The following office action is in response to the Request for Continued Examination, filed on January 4, 2007. Claims 1, 4-21 are pending. Claims 1, 5, and 10 are amended. Claims 18-21 are newly added. Claims 2 and 3 have been cancelled.

Claim Objections

1. Claims 4-6 are objected to because of the following informalities: Claim 4 is shown to be dependent upon claim 2 which has been cancelled. Appropriate correction is required.

With respect to claim 5 and 6, these claims depend upon claim 4 which further depends upon a cancelled claim. Appropriate correction is required.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 1, 4-21 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

With respect to claim 1, applicant amends claim 1 to recite, "the second signal wire being directly connected to the ground through a resistor". The limitation of "being directly connected to the ground through a resistor" is indefinite. The second signal wire cannot be *directly* connected to the ground if it is connected *through* a resistor. Appropriate correction is required.

With respect to claim 10, applicant amends claim 10 to recite, "the second shift clock signal wire being directly connected to a ground through a resistor". The limitation of "being directly connected to a ground through a resistor" is indefinite. The second shift clock signal

wire cannot be *directly* connected to a ground if it is connected *through* a resistor. Appropriate correction is required.

Claims 4-9, 11-21 are rejected as being indefinite as they depend upon indefinite claims.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1, 4-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Misawa et al (US 5,811,837) in view of Garlepp et al (US 6,198,307).

As to independent claim 1, Misawa et al disclose a liquid crystal display system comprising, a liquid crystal display (Fig. 1) including a plurality of data lines (Fig. 1, items 26-28), a plurality of gate lines (Fig. 1, items 24 and 25) intersecting the data lines and a plurality of pixel electrodes (Fig. 1, items 32 and 33) arranged in a matrix type and each having a switch connected to one of the gate lines and one of the data lines (col. 4, lines 50-64); a gate driver (Fig. 1, item 21, col. 4, lines 35-40) for successively applying a gate voltage to the gate lines to turn on the switches; a data driver (Fig. 1, item 12, col. 4, lines 35-40) for applying a gray voltage, corresponding to image data signals to the data lines;

Misawa et al disclose clock signals which are 180 degrees out of phase as shown in Fig. 11, and col. 12 lines 13-34. Misawa et al does not disclose a timing controller for sending both the image data signals and a shift clock signal to the data driver, with a first signal wire through which the shift clock signal is transmitted. Garlepp et al disclose a timing controller for sending

both the image data signals and a shift clock signal to the data driver, with a first signal wire through which the shift clock signal is transmitted in Fig. 9, item 15, and col. 7, lines 12-37. Garlepp et al teach where the first and second signal wires are formed in parallel in Fig. 13. It would have been obvious to one of ordinary skill in the art to incorporate the timing controller of Garlepp et al into that of Misawa et al as they both disclose clock signals for a liquid crystal display as Misawa et al would have a timing controller similar to that of Garlepp and also, the timing controller would have been outputting the timing signals (col. 4, lines 59-64 of Garlepp).

Misawa et al disclose a second signal wire through which a first clock signal having a frequency equal to the shift clock signal but having a phase difference of 90 to 270 degrees (Fig. 11, items 2 and 9, and col. 12, lines 13-34). Misawa et al does not disclose where the second signal wire is transmitted to ground. Garlepp et al disclose in Fig. 9, items CTMN, and col. 7, line 38-col. 8, line 4, where the second signal wire (CTMN) is connected to ground. It would have been obvious to one of ordinary skill in the art that this feature of the second signal wire connected to ground as shown by Garlepp could have been incorporated into that of Misawa et al as Misawa does not show where the end of the signal wire leads and thus could have been interpreted to be similar to that of Garlepp et al. The second signal wire connected to ground is advantageous as it enables the display to reduce noise (col. 4, lines 59-64 of Garlepp).

Since the applicant has failed to disclose that having the second signal wire connected through a predetermined resistance value provides an advantage, is used for a particular purpose, or solves a stated problem, it is an obvious matter of design choice to have such a configuration in Garlepp. Therefore, it would have been obvious to use a capacitor, since the capacitor would

perform equally well at grounding the wire in order to reduce noise (col. 4, lines 59-64 of Garlepp).

As to independent claim 10, limitations of claim 1, and further comprising, Misawa et al disclose a circuit board (Fig. 15). Misawa et al do not disclose a timing controller for generating a first image data signal and a second image data signal and generating a first shift clock signal and a second clock signal with a phase difference of 90 to 270 degrees that respectively shift the first image data signal and the second image data signal a first image data signal wire and a second image data signal wire through which the first image data signal and the second image data signal are respectively transmitted.

Garlepp et al disclose a timing controller for generating a first image data signal and a second image data signal and generating a first shift clock signal and a second clock signal with a phase difference of 90 to 270 degrees that respectively shift the first image data signal and the second image data signal, a first image data signal wire and a second image data signal wire through which the first image data signal and the second image data signal are respectively transmitted in Fig. 9, item 15, and col. 7, lines 12-37. It would have been obvious to one of ordinary skill in the art to incorporate the timing controller of Garlepp et al into that of Misawa et al as they both disclose clock signals for a liquid crystal display as Misawa et al would have a timing controller similar to that of Garlepp and also, the timing controller would have been outputting the timing signals (col. 4, lines 59-64 of Garlepp).

Misawa et al disclose a data driver (Fig. 1, item 12) receiving the first image data signal and the second image data signal and the first shift clock signal and the second shift clock signal from the timing controller (Fig. 1, items 32 & 35, col. 4, lines 36-col. 5, line 5) and applying a

gray voltage corresponding to the first image data signal and the second image data signal to the data lines shown by col. 4, lines 36-col. 5, line 5.

Garlepp et al disclose wherein the second signal wire is connected to said ground in Fig. 9, items CTMN through a capacitor, and col. 7, line 38-col. 8, line 4, where the second signal wire (CTMN) is connected through a capacitor to ground. Since the applicant has failed to disclose that having the second signal wire connected through a predetermined resistance value provides an advantage, is used for a particular purpose, or solves a stated problem, it is an obvious matter of design choice to have such a configuration in Garlepp. Therefore, it would have been obvious to use a capacitor, since the capacitor would perform equally well at grounding the wire in order to reduce noise.

As to dependent claim 4, limitations of claim 2, and further comprising, Misawa et al disclose wherein the first signal wire and the second signal wire are provided on a circuit board as shown by Fig. 3a-3b, 4a-4d.

As to dependent claims 5 and 6, limitations of claim 4, and further Misawa et al and Garlepp et al do not explicitly state the signal wires are on the same layer or a different layer. Examiner takes official notice that having signal wires formed on the same layer or a different layer is well known in the art. It would have been obvious to one of ordinary skill in the art at the time the invention was made to include the features of where the signal wires are on the same layer or a different layer as being formed on the same layer reduces the size of the display construction and where the signal wires are formed on a different layer enables an active matrix LCD where higher image quality is provided.

As to dependent claim 7, limitations of claims 1 and 10, and further comprising, Misawa et al discloses wherein the first clock signal has a 180 degree phase difference from the shift clock as shown in Fig. 11, and col. 12 lines 13-34.

As to dependent claim 8, limitations of claim 7, and further comprising, Misawa et al disclose wherein the data driver comprises a plurality of data driver integrated circuits for receiving the image data signals and the shift clock signal from the timing controller and applying the gray voltage corresponding to the image data signals to the data lines of the LCD panel as shown in Figs. 1, 2a-2e, col. 4, lines 36-64 and col. 5, lines 37-62.

As to dependent claim 9, limitations of claim 8, and further comprising Misawa et al disclose wherein the data driver integrated circuits comprise a shift register (Fig. 8, item 163), a D/A converter receiving the image data signals stored in the shift register and converting the image data signals to a corresponding gray voltage and an output buffer for temporarily storing the gray voltage from the D/A converter and applying the voltage to the data lines of the liquid crystal display. Misawa et al disclose a sampling transistor circuit (Fig. 8, item 166) is shown to receive the image data signals which are stored in the shift register and convert the signals and apply the voltage to the data lines of the lcd as shown in col. 11, lines 1-22.

As to dependent claim 11, limitations of claim 10, and further comprising Misawa et al disclose wherein the first data signals are odd image data signals, and the second image data signals are even image data signals (col. 4, lines 35-64).

As to dependent claim 12, limitations of claim 10, and further comprising, Misawa et al disclose wherein the first shift clock signal and the second shift clock signal have a phase difference of 180 degrees (Fig. 11, and col. 12 lines 13-34).

As to dependent claim 13, limitations of claim 12, and further comprising, Misawa et al teach wherein the first image data signal and the second image data signal have a phase difference of 90 to 270 degrees (Fig. 13).

As to dependent claim 14, limitations of claim 13, and further comprising, Misawa et al disclose wherein the first image data signal and the second image data signal have a phase difference of 180 degrees (Fig. 11, and col. 12 lines 13-34).

As to dependent claim 15, limitations of claim 14, and further comprising, Misawa et al disclose wherein the first image data signal is synchronized to a rising edge of the first shift clock signal and the second image data signal is synchronized to a falling edge of the second shift clock signal (Fig. 11 and 13, and col. 12 lines 13-34).

As to dependent claim 16, limitations of claim 14, Misawa et al disclose wherein a pulse width of the first shift clock signal and the second shift clock signal falls within the interval of a high signal or a low signal of the odd image data signal and the even image data signal (Fig. 11, and col. 12 lines 13-34).

As to dependent claim 17, limitations of claim 13, and further comprising, Misawa et al disclose wherein the first image data signal and the second image data signal have a phase difference of 90 to 270 degrees (Fig. 13).

As to dependent claim 18, limitations of claim 1, and further comprising, Misawa et al do not teach wherein the first clock signal transmitted to the ground is effective to offset electromagnetic interference (EMI) caused by the transmission of the shift clock signal.

Garlepp et al disclose in Fig. 9, items CTMN, and col. 7, line 38-col. 8, line 4, where the first clock signal (CTMN) is connected to ground. It would have been obvious to one of

ordinary skill in the art that this feature of the first clock signal connected to ground as shown by Garlepp could have been incorporated into that of Misawa et al as Misawa does not show where the end of the signal wire leads and thus could have been interpreted to be similar to that of Garlepp et al. The second signal wire connected to ground is advantageous as it enables the display to reduce noise (col. 4, lines 59-64 of Garlepp). This reduction of noise as disclosed by Garlepp is consistent with the offset of electromagnetic interference caused by the transmission of the shift clock.

As to dependent claim 19, limitations of claim 18, and further comprising, Garlepp et al teach in Fig. 9, items CTMN and col. 7, lines 38-col. 8, line 4, wherein the ground has a ground surface, the first clock signal transmitted to the ground being effective to reduce current fluctuation on the ground surface (i.e. reduction of noise, col. 4, lines 59-64 of Garlepp).

As to dependent claim 20, limitations of claim 10, and further comprising, Misawa does not teach wherein the second shift clock signal transmitted to the ground is effective to offset electromagnetic interference (EMI) caused by the transmission of the first shift clock signal. Garlepp et al disclose in Fig. 9, items CTMN, and col. 7, line 38-col. 8, line 4, where the second shift clock signal (CTMN) is connected to ground. It would have been obvious to one of ordinary skill in the art that this feature of the second shift clock signal connected to ground as shown by Garlepp could have been incorporated into that of Misawa et al as Misawa does not show where the end of the signal wire leads and thus could have been interpreted to be similar to that of Garlepp et al. The second signal wire connected to ground is advantageous as it enables the display to reduce noise (col. 4, lines 59-64 of Garlepp). This reduction of noise as disclosed

by Garlepp is consistent with the offset of electromagnetic interference caused by the transmission of the first shift clock signal.

As to dependent claim 21, limitations of claim 20, and further comprising, Garlepp et al teach in Fig. 9, items CTMN and col. 7, lines 38-col. 8, lines 4, wherein the ground has a ground surface, the first shift clock signal transmitted to the ground being effective to reduce current fluctuation on the ground surface (i.e. reduction of noise, col. 4, lines 59-64 of Garlepp).

Response to Arguments

6. Applicant's arguments filed January 4, 2007 have been fully considered but they are not persuasive.

Please see the 35 USC 112, second paragraph rejection above.

Applicant argues where the prior art of Misawa and Garlepp, either singularly or in combination fail to teach "the second signal wire being directly connected to the ground through a resistor, the first clock signal being generated in the timing controller, the first signal wire and the second signal wire being formed in parallel". Examiner, respectfully, disagrees. Misawa et al disclose clock signals which are 180 degrees out of phase as shown in Fig. 11, and col. 12 lines 13-34. Garlepp et al disclose a timing controller for sending both the image data signals and a shift clock signal to the data driver, with a first signal wire through which the shift clock signal is transmitted in Fig. 9, item 15, and col. 7, lines 12-37. Garlepp et al teach where the first and second signal wires are in parallel in Fig. 13. With respect to where the second signal wire being directly connected to the ground through a resistor, Garlepp et al disclose wherein the second signal wire is connected to said ground in Fig. 9, items CTMN through a capacitor, and col. 7, line 38-col. 8, line 4, where the second signal wire (CTMN) is connected through a

capacitor to ground. Since the applicant has failed to disclose that having the second signal wire connected through a predetermined resistance value provides an advantage, is used for a particular purpose, or solves a stated problem, it is an obvious matter of design choice to have such a configuration in Garlepp. Therefore, it would have been obvious to use a capacitor, since the capacitor would perform equally well at grounding the wire in order to reduce noise.

With respect to applicant's arguments in regards to the feature "in order to reduce electromagnetic interference (EMI)", this is accomplished as taught by Garlepp et al in the form of noise reduction.

With respect to applicant's arguments in regards to claim 10, as they are the same as the arguments of claim 1, applicant is directed to the above explanation.

With respect to newly added claims 18-21, see rejection above.

Therefore, as shown above, the combination of Misawa et al in view of Garlepp disclose the claimed invention.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Srilakshmi K. Kumar whose telephone number is 571 272 7769. The examiner can normally be reached on 9:00 am to 5:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sumati Lefkowitz can be reached on 571 272 3638. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Srilakshmi K. Kumar
Examiner
Art Unit 2629

SKK
March 27, 2007

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